REMARKS

By the present amendment and response, independent claims 1 and 14 and dependent claims 1, 4-5, 12, 14, 17, 20 and 23 have been amended to overcome the Examiner's objections. Reconsideration and allowance of pending claims 1-15 and 17-25 in view of the following remarks are requested.

A. Objection to Claims 1, 9, 12, 20 and 23 due to Informalities

The Examiner has objected to claims 1, 9, 12, 20, and 23 because of informalities. In particular, the Examiner has stated that the singular term "region" in claim 1 should be replaced with the plural term "regions." To overcome the objection, Applicant has amended claim 1 to recite a "transistor gate region" and a "field oxide region". Dependent claims 4-5 have been amended to recite a "transistor gate region". Accordingly, Applicant respectfully submits that objection of claim 1 has been traversed.

The Examiner has further objected to the use of a "*" symbol in claims 9, 12, 20, and 23 to indicate a multiplication operation. To overcome the objection, Applicant has amended claims 9, 12, 20, and 23 to recite an "x" symbol to indicate a multiplication operation. Accordingly, Applicant respectfully submits that objection of claims 9, 12, 20, and 23 has been traversed.

B. Rejection of Claims 1, 14 and 17 under 35 U.S.C. § 112

The Examiner has rejected claims 1, 14 and 17 under 35 USC §112 as containing subject matter which was not described in the specification. Although Applicant respectfully disagrees with the Examiner's rejection, in order to expedite allowance of the

present application, Applicant has amended independent claims 1, 14 and 17 to delete the term "overdoping" in response to the Examiner's rejection. Accordingly, Applicant respectfully submits that rejection of claims 1, 14 and 17 has been traversed.

C. **Rejection of Claims 1, 3, 6-12 and 14-23 under 35 U.S.C. § 102(b)**

The Examiner has rejected claims 1, 3, 6-12 and 14-23 under 35 USC §102(b) as being anticipated by **Zaccherini** (USPN 5,436,177) ("**Zaccherini '177**"). Although Applicant respectfully disagrees with the Examiner's rejection, in order to expedite allowance of the present application, Applicant has amended independent claims 1 and 14 in response to the Examiner's rejection. For the reasons discussed below, Applicant respectfully submits that amended independent claims 1 and 14 and dependent claims 3, 6-12, 15 and 17-20, are patentably distinguishable over **Zaccherini '177**.

The present invention is directed to low cost fabrication of high resistivity resistors. The invention provides an economical and simplified method for formation of high resistivity resistors in large scale integrated CMOS processes which is compatible with the formation of polycrystalline silicon gates in PFETs and NFETs. The invention reduces cost by providing a resistor fabrication process which does not rely on the use of multiple doping barriers to form the implant doped portion of a high resistivity resistor. Moreover, fabrication of high resistivity resistors with improved temperature coefficient and more accurate control of resistivity value is facilitated.

As recited in amended independent claim 1, the invention's method includes steps of "forming a layer over a transistor gate region and a field oxide region; forming a

doping barrier above said layer over said field oxide region; doping said layer over said transistor gate region with a dose of a first dopant, wherein said dose of said first dopant is a dosage greater than required to result in said layer over said transistor gate region having transistor gate electrical properties; removing said doping barrier; doping said layer over said transistor gate region and said field oxide region with a second dopant so as to form a high resistivity resistor in said layer over said field oxide region without affecting said transistor gate electrical properties."

With regard to independent claim 1, **Zaccherini '177** fails to disclose, teach or suggest the above recited limitations specified by claim 1. **Zaccherini '177** discloses a method of manufacturing semiconductor devices by first placing a masking layer over areas 8 of polycrystalline layer 7 where P-doped resistors will be formed, and implanting an N-type dopant having a high atomic weight in unmasked areas of polycrystalline layer 7. See, for example, column 3, lines 15-21 and Figure 4 of **Zaccherini '177**. In **Zaccherini '177**, the N-type dopant implant provides selective pre-amorphousization of areas of polycrystalline layer 7 that might be affected by the channeling phenomenon, such as amorphousized zone 12 of the polycrystalline layer 7. See, for example, column 3, lines 33-38 and lines 54-62. In **Zaccherini '177**, the contemplated dosage of N-type dopant is in the range $5x10^{14}$ to $1x10^{16}$ ions/cm2. See, for example, column 3, lines 29-31. In addition to pre-amorphousization of the selected areas, the N-type dopant implant step allows the gate region of the semiconductor device to be doped. See, for example, column 3, lines 38-39. Next, the mask is removed and a medium to low dosage, e.g.

between $1x10^{12}$ and $1x10^{15}$ ions/cm2, of a P-type dopant is applied across the entire wafer to form resistors in areas 8 of polycrystalline layer 7. See, for example, column 3, lines 44-58 and Figure 6. Thus, **Zaccherini '177** teaches forming resistors in areas 8 of polycrystalline layer 7 by a medium to low dosage, e.g. between $1x10^{12}$ and $1x10^{15}$ ions/cm2, of P-type dopant. In contrast, amended claim 1 recites doping with a second dopant so as to form a high resistivity resistor.

Moreover, **Zaccherini '177** teaches a N-type dopant implant step that only enables the gate region of the semiconductor device to be doped. In contrast, amended claim 1 recites "doping with a dose of a first dopant, wherein said dose of said first dopant is a dosage greater than required to result in said layer over said transistor gate region having transistor gate electrical properties; and doping with a second dopant without affecting said transistor gate electrical properties." Thus, **Zaccherini '177** does not teach or suggest doping with a first dopant to result in a gate region having transistor gate electrical properties that are unaffected after doping with a second dopant due to the dose of the first dopant being greater than required to result in the gate region having transistor gate electrical properties.

Independent claim 14 has been amended to include the limitations recited in amended independent claim 1. Thus, based on the reasons described above with regard to claim 1, independent claim 14 is patentable over **Zaccherini '177**. Pending claims 3, 6-12, 15 and 17-20 are allowable because they depend from either claims 1 or 14, which are patentable over **Zaccherini '177**.

D. Rejection of Claims 2, 4-5, 13, and 24-25 under 35 U.S.C. § 103(a)

The Examiner has also rejected claims 2, 4-5, 13, and 24-25 as being unpatentable over **Zaccherini '177** in view of **Liu et al.** (USPN 6,165,861) ("**Liu '861**"). As discussed above, amended independent claims 1 and 14 are patentably distinguishable over **Zaccherini '177** and, as such, claims 2, 4-5, and 13 depending from amended independent claim 1 and claims 24-25 depending from amended independent claim 14 are, *a fortiori*, also patentably distinguishable over **Zaccherini '177**. Moreover, the features of amended independent claims 1 and 14, for example, "doping with a dose of a first dopant, wherein said dose of said first dopant is a dosage greater than required to result in said layer over said transistor gate region having transistor gate electrical properties; and doping with a second dopant without affecting said transistor gate electrical properties," are not suggested, disclosed, or taught anywhere in **Liu '861**. As such, amended independent claim 1 and dependent claims 2, 4-5, and 13, and amended independent claim 14 and dependent claims 24-25 are also patentably distinguishable over **Zaccherini '177** in combination with **Liu '861**.

E. Conclusion

Based on the foregoing reasons, amended independent claim 1 and 14 and claims depending therefrom, are patentably distinguishable over the art cited by the Examiner. Thus, claims 1-15 and 17-25 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1-15 and 17-25 pending in the present application is respectfully requested.

Respectfully Submitted,
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Version with Markings to Show Changes Made

In the Claims:

Claims 1, 4-5, 9, 12, 14, 17, 20, and 23 have been amended as follows:

1. (Twice Amended) A method comprising steps of:

forming a layer over a transistor gate region and a field oxide region;

forming a doping barrier above said layer over said field oxide region;

[overdoping with a first dopant] doping said layer over said transistor gate region with a dose of a first dopant, wherein said dose of said first dopant is a dosage greater than required to result in said layer over said transistor gate region having transistor gate electrical properties;

removing said doping barrier;

doping said layer over said transistor gate region and said field oxide region with a second dopant so as to form a high resistivity resistor in said layer over said field oxide region without affecting said transistor gate electrical properties.

4. (Once Amended) The method of claim 1 wherein said transistor gate region is a gate of an PFET.

5. (Once Amended) The method of claim 1 wherein said transistor gate region is a gate of an NFET.

9. (Once Amended) The method of claim 1 wherein said first dopant comprises phosphorous at a dose of approximately [$6.5*10^{15}$] $6.5x10^{15}$ atoms per square centimeter.

12. (Once Amended) The method of claim 1 wherein said second dopant comprises boron at a dose of approximately [$1.0*10^{15}$] $1.0x10^{15}$ atoms per square centimeter.

14. (Twice Amended) A method comprising steps of:

depositing a polycrystalline silicon layer on a chip, said polycrystalline silicon layer including a gate region and a resistor region;

forming a doping barrier above said polycrystalline silicon layer so as to prevent doping of said resistor region of said polycrystalline silicon layer;

[overdoping] doping said polycrystalline silicon layer with a dose of a first dopant, wherein said dose of said first dopant is a dosage greater than required to result in said layer over said gate region having transistor gate electrical properties;

removing said doping barrier;

doping said polycrystalline silicon layer with a second dopant so as to form a high resistivity resistor in said resistor region of said polycrystalline silicon layer without affecting said transistor gate electrical properties.

17. (Twice Amended) The method of claim 14 wherein said step of [overdoping] doping said polycrystalline silicon layer with a first dopant comprises [overdoping] doping said gate region.

20. (Once Amended) The method of claim 14 wherein said first dopant comprises phosphorous at a dose of approximately [$6.5*10^{15}$] $6.5x10^{15}$ atoms per square centimeter.

23. (Once Amended) The method of claim 14 wherein said second dopant comprises boron at a dose of approximately [$1.0*10^{15}$] $1.0x10^{15}$ atoms per square centimeter.